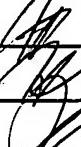
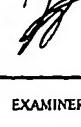
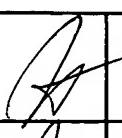
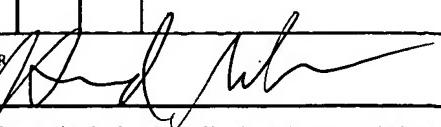


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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)			APPLICANT Luan Tran et al.				
			FILING DATE Filed Herewith		GROUP		
U.S. PATENT DOCUMENTS							
*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,045,899	09/03/91	Arimoto			
	AB	5,107,459	04/21/92	Chu et al.			
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	AE	5,537,347	07/16/96	Shiratake et al.			
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	AJ	5,747,844	05/05/98	Aoki et al.			
	AK	5,665,623	09/09/97	Liang et al.			
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							Yes
	AL	JP 03205868	09/09/91	Japan			Abs.
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	A. Chatterjee et al., "A Shallow Trench Isolation Study for 0.25/0.18 μ m CMOS Technologies and Beyond", IEEE, 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996).					
	AS	M. Aoki et al., "Fully Self-Aligned 6F ² Cell Technology for Low Cost 1Gb DRAM", IEEE 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 22-23 (1996).					
	AT	J.S. KIM et al., "A Triple Level Metallization Technique for Gigabit Scaled DRAMS", VMIC CONFERENCE, Technology Development, Memory Device Business, Samsung Electronic Co., pp. 28-33 (June 18-20, 1996).					
EXAMINER			DATE CONSIDERED				
<i>[Signature]</i>			9/17/04				
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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*Examiner Initial		Document Number	Date	Name	Class Subclass Filing Date If Appropriate		
	AA-	5,637,528	06/10/97	Higashitani et al.			
	AB	5,756,390	5/26/1998	Juengling et al.			
	AC	5,736,670	4/7/1998	Carbonell et al.			
	AD						
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		Document Number	Date	Country	Class Subclass	Translation	
						Yes	No
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	AR		B. KEETH, "A Novel Architecture for Advanced High Density Dynamic Random Access Memories".				
			A Thesis for M.S. E.E., University of Idaho pp. 1-62 (i-vi). (May 1996).				
	AS		T. Hamamoto et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 Mb DRAM and Beyond".				
			IEICE Transactions On Electronics, pp. 789-796, 1995.				
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FOREIGN PATENT DOCUMENTS						Translation		
		Document Number	Date	Country	Class			Subclass
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	AO							
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	AQ							
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		SSDM '95 - Device and Process Technology, 2 pages.						
	AS	Fazen, et al., "A High-C Capacitor (20.4fF/μ ²) with Ultrathin CVD-Ta _x O _y films Deposited on Rugged Poly-Si for High Density DRAMs": 1992; 4 pps.						
	AT	Fazen et al., "A Highly Manufacturable Trench Isolation Process for Deep Submicron DRAMs," ©1993 IEEE, 4 pages.						
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